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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/034,227	12/28/2001	Timothe Litt	1662-53000 JMH (P01-3850)	9091

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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/034,227	LITT, TIMOTHE	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *65-76 and 78-85* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *80-85* is/are allowed.

6)☒ Claim(s) *65-73,75,78 and 79* is/are rejected.

7)☒ Claim(s) *74 and 76* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a FINAL Office Action in response to AMENDMENT filed 12/27/2005.

Claims 65-85 were previously examined. Claim 77 has been cancelled.

Claims 65-76 and 78-85 are pending.

Objection to the drawings of Figure 1 in the prior Office Action under 37 CFR 1.83(a) has been withdrawn in view of replacement drawing sheets in compliance with 37 CFR 1.121(d) including corrections as required by the Office Action.

Response to Amendment

The amendment filed 12/27/2005 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure, 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: In paragraph [0009] of the original Specification, "a history buffer or an on-chip logic analyzer (OCLA) of one type or another is" provided to acquire and store event and/or time sequenced data on the chip itself. Applicant is required to cancel the new matter in the reply to this Office Action.

Response to Arguments

Applicant's arguments filed 12/27/2005 have been fully considered but they are not persuasive.

In response to Applicant's argument, with respect to rectifying the error of teaching or suggesting the use of multiple on-chip logic analyzers on a single chip as a

prior art, the Examiner notes that Applicant's amendment of paragraph [0009] of the original specification of using only one on-chip logic analyzer (OCLA) on a single chip, amounts to a new matter in the disclosure because the added material is not supported by the original disclosure.

Regarding Claim independent claim 65, the Examiner agrees with the Applicant's argument that the cited reference by Arimilli fails to teach "multiple on-chip logic analyzers" on an integrated circuit. However, as described in the Office Action, Applicant's Admitted Prior Art in the original disclosure paragraph [0009] suggests "multiple on-chip logic analyzers" by stating that "on-chip logic analyzers (OCLA) are provided to acquire and store event and/or time sequenced data on the chip itself".

Applicant's further argues that the presence of multiple on-chip logic analyzers becomes practicable, because the disclosed word recognizer can be implemented with a minimum of logic, providing a great deal of flexibility while consuming a relatively small amount of chip space. However, the features cited by Applicant's arguments are not part of the claims. In response to applicant's argument, it is noted that the features upon which applicant relies (i.e., minimum of logic with great deal of flexibility) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960), although the Arimilli reference does not disclose a "multiple on-chip logic analyzers", the mere duplication of identical on-chip logic analyzers fails to produce new and unexpected results, since the

logic analyzers are identical, as shown in the replacement Figure 1 of the instant application, and as such the fabrication of "multiple on-chip logic analyzers" on a chip does not carry a patentable weight.

In response to applicant's argument that it is not reasonable and therefore not obvious to merely duplicate identical on-chip logic analyzers, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to duplicate "on-chip logic analyzers" on the VLSI circuit of Arimilli, as taught by Applicant's Admitted Prior Art and as cited in Harza, thereby reducing the problems of interfacing slower speed test equipment with high-speed devices. Furthermore, a person skilled in the art would have been motivated to do so, since the incorporation of a plurality of "on-chip logic analyzers" results in improving high-speed parallel processing for the high-speed data generated on the chip.

Regarding independent Claim 78 as currently amended, in response to Applicant's argument with respect to the claimed limitation of "multiple on-chip logic analyzers", claim 78 is still rejected as being obvious under 35 U.S.C. 103(a) for the same response to arguments as described in reference to Claim 65.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 65-73, 75, 78, 79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,633,838) in view of Applicant's Admitted Prior Art, and further in view of in re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

Regarding independent Claim 65, Arimilli substantially discloses an integrated circuit (VLSI circuit 100) fabricated on a chip, comprising:

An on-chip logic analyzer (multi-state logic analyzer 120) including a trigger word recognizer (condition select logic 150), Figure 1.

An on-chip memory (array 140) capable of storing data selected by the trigger word recognizer (150), wherein the trigger word recognizer (150) includes a Boolean logic section (logical XNOR and OR operation, Figures 4 and 5) and a counter/timer section including a (counter 670, Figure 6) located on-chip.

Arimilli does not explicitly disclose "multiple on-chip logic analyzers" on an integrated circuit. However, in the Background of the Invention, Applicant's Admitted Prior Art discloses "multiple on-chip logic analyzers" by stating that "on-chip logic

analyzers (OCLA) are provided to acquire and store event and/or time sequenced data on the chip itself", which is an alternative to sending data off-chip, thereby reducing the problems of interfacing slower speed test equipment with high-speed devices. Furthermore, in re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960) the court held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced. In this case, although the Arimilli reference does not disclose a "multiple on-chip logic analyzers", the mere duplication of identical on-chip logic analyzers produces identical results.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a plurality of "on-chip logic analyzers" on the VLSI circuit of Arimilli, as taught by Applicant's Admitted Prior Art and as cited in Harza, thereby reducing the problems of interfacing slower speed test equipment with high-speed devices. Furthermore, a person skilled in the art would have been motivated to do so, since the incorporation of a plurality of "on-chip logic analyzers" results in improving high-speed parallel processing for the high-speed data generated on the chip.

Regarding Claim 66, Arimilli substantially discloses (Figures 1, 4 and 5) a multi-state logic analyzer 120 including a plurality of software match logical units (XNOR and OR) using (programmable pattern 405, 410 or 415) and programmable don t care mask, (420, 425, or 430), which are capable of detecting a software event, and which produce match signals TRIGGERS (435, 440, or 445).

Arimilli does not explicitly disclose that, "the match signals are each available as a condition to at least one other on-chip logic analyzer". However, as described in

claim 65, Applicant's Admitted Prior Art discloses that "on-chip logic analyzers (OCLA) are provided to acquire and store event and/or time sequenced data on the chip itself". Therefore, claim 66 is rejected for the same obvious and motivational reasons as applied in the independent claim 65 above.

Regarding Claim 67, Arimilli discloses wherein the match signals (TRIGGERS) generated from the trace data control logic 130 is available for capture by the on-chip memory (trace array 140). The trace data control logic 130 controls the state of the trace array 140 and generates triggers based on comparisons to programmable trigger criteria, Figure 1.

Regarding Claim 68, Arimilli discloses wherein the match signals (TRIGGERS) are each provided as an output of the chip through the trace array input and output logic (160), which is accessible at both the wafer and component stage to allow for testing and debugging of the VLSI circuitry, Figure 1.

Regarding Claim 69, Arimilli discloses wherein the multi-state logic analyzer 120 analyzer includes a storage word recognizer (trace data control logic 130).

Regarding Claim 70, Arimilli discloses wherein the storage word recognizer (trace data control logic 130) controls the state of the trace array 140 for storing data, using the input and output logic 160, which allows reading or writing from or to the trace array 140, and programming of trigger and condition criteria for transitioning states within the logic analyzer 120.

Regarding Claims 71, Arimilli discloses the trigger word recognizer (150) including a Boolean logic section (logical XNOR and OR operation, Figures 4 and 5)

and a counter/timer section including a (counter 670, Figure 6) located on-chip. Arimilli further discloses a Boolean logic section (Figures 4 and 5) including a plurality of hardware match logical units (XNOR and OR) using (programmable pattern 405, 410 or 415) and programmable don t care mask, (420, 425, or 430), which are capable of detecting a software event, and which produce a true output signal TRIGGER (435, 440, or 445). Furthermore, the Boolean logic section permits a user to enable one or more individual hardware match logical units (XNOR and OR) by controlling the event data from the trace data control logic 130, as shown in Figure 1.

Regarding Claim 72, Arimilli discloses in a trigger word recognizer (condition select logic 150, Figures 1 and 5), the conditions are met by comparing each one of a plurality of triggers, (500, 505, 510, 515, 520, or 525) to a condition trigger mask 530 by a bit-wise logical AND (535, 540, 545, 550, 555, or 560). The results of each logical AND operation are then passed through a bit-wise logical OR 565, so that if any trigger matches the condition trigger mask 530, the condition will be met 570.

Regarding Claim 73, Arimilli discloses wherein the output of the AND gates (535, 540, 545, 550, 555, or 560) and the output of the OR gate 565 are combined together in 570 when the condition is met.

Regarding Claims 75, Arimilli discloses trigger word recognizer (150) including a Boolean logic section (Figures 4 and 5) including a plurality of software match logical units (XNOR and OR) using (programmable pattern 405, 410 or 415) and programmable don t care mask, (420, 425, or 430), which are capable of detecting a software event, and which produce a true output signal TRIGGER (435, 440, or 445).

Furthermore, the Boolean logic section permits a user to enable one or more individual software match logical units (XNOR and OR) by controlling the event data from the trace data control logic 130, as shown in Figure 1.

Regarding independent Claim 78, Arimilli substantially discloses an integrated circuit (VLSI circuit 100) fabricated on a chip, comprising:

An on-chip logic analyzer (multi-state logic analyzer 120) that comprises a trigger word recognizer (condition select logic 150) and a storage word recognizer (trace data control logic 130) Figure 1.

An on-chip memory (array 140) that captures data from the (input and output logic 160) determined by the storage word recognizer (trace data control logic 130) in response to a match signal (MATCH TRIGGER) from the trigger word recognizer (150), as illustrated in Figure 1, and describes as follows: "The input and output logic 160 allows reading or writing from or to the trace array 140, and programming of trigger and condition criteria for transitioning states within the logic analyzer 120. The trace data control logic 130 preferably controls the state of the trace array 140 and generates triggers based on comparisons to programmable trigger criteria" (Col. 4, lines 45-60).

The on-chip logic analyzer (multi-state logic analyzer 120) comprises a trigger word recognizer (condition select logic 150) and a storage word recognizer (trace data control logic 130) Figure 1.

Arimilli does not explicitly disclose "multiple on-chip logic analyzers" on an integrated circuit. However, in the Background of the Invention, Applicant's Admitted Prior Art discloses "multiple on-chip logic analyzers" by stating that "on-chip logic

analyzers (OCLA) are provided to acquire and store event and/or time sequenced data on the chip itself", which is an alternative to sending data off-chip, thereby reducing the problems of interfacing slower speed test equipment with high-speed devices. Furthermore, in re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960) the court held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced. In this case, although the Arimilli reference does not disclose a "multiple on-chip logic analyzers", the mere duplication of identical on-chip logic analyzers produces identical results.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a plurality of "on-chip logic analyzers" on the VLSI circuit of Arimilli, as taught by Applicant's Admitted Prior Art and as cited in Harza, thereby reducing the problems of interfacing slower speed test equipment with high-speed devices. Furthermore, a person skilled in the art would have been motivated to do so, since the incorporation of a plurality of "on-chip logic analyzers" results in improving high-speed parallel processing for the high-speed data generated on the chip.

Regarding Claim 79, Arimilli substantially discloses (Figures 1, 4 and 5) a multi-state logic analyzer 120 including a plurality of software match logical units (XNOR and OR) using (programmable pattern 405, 410 or 415) and programmable don t care mask, (420, 425, or 430), which are capable of detecting a software event, and which produce match signals TRIGGERS (435, 440, or 445).

Arimilli does not explicitly disclose that, "the match signals are each available as a condition to at least one other on-chip logic analyzer". However, as described in

claim 78, Applicant's Admitted Prior Art discloses that "on-chip logic analyzers (OCLA) are provided to acquire and store event and/or time sequenced data on the chip itself". Therefore, claim 79 is rejected for the same obvious and motivational reasons as applied in the independent claim 78 above.

Allowable Subject Matter

Claims 80-85 are allowed.

The following is an examiner's statement of reasons for allowance: The prior arts of record taken alone or in combination fail to teach, anticipate, suggest or render obvious the claimed invention, as recited in the independent claim 80, and integrated circuit fabricated on a chip including "word recognizers each comprise a Boolean logic section and a counter/timer section, wherein the Boolean logic section includes multiple hardware match logical units that compare a match value with internal state data and produce an output signal that is true if the comparison indicates a match condition, and wherein each the output signal of the hardware match logical units connects to both an AND term and an OR term, and a user selects whether the AND term or the OR term is enabled for each of the hardware match logical units".

Consequently, claims 80-85 are allowed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Claims 74, 76, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior arts of record taken alone or in combination fail to teach, anticipate, suggest or render obvious the claimed invention as recited in claims 74 and 76.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2138

By: _____

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Office Action: Final Rejection

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